**实验十三：计数器/定时器设计与应用**

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| 实验时间： | 2015-12-周三 | | 实验地点： | 紫金港东4-509 | | 指导老师： | | 蒋方炎，王总辉 |

**设计工程一：Exp130-WallClock**

1：用verilog设计实现毫秒计数器

module millisecond(

input clk,

input reset,

output clk\_1ms

);

parameter COUNTER=16;

reg [COUNTER-1:0]count;

reg second\_m;

initial count<=0;

always@(posedge clk)

begin

if(!reset||(count[COUNTER-1:0]==49999))

begin

count[COUNTER-1:0]<=0;

second\_m<=1;

end

else

begin

count[COUNTER-1:0]<=count+1;

second\_m<=0;

end

end

assign clk\_1ms=second\_m;

Endmodule

以毫秒计数器为依据，设计秒计数器：

module clk\_1ms(

input clk,

input reset,

output reg clk\_1s,

output [11:0] msecond

);

reg [11:0] mss;

initial begin

mss <=0;

end

assign msecond=mss;

always@(posedge clk)

begin

if(!reset)

begin

mss<=0;

clk\_1s<=0;

end

else if(mss==12'b100110011001)

begin

mss<=0;

clk\_1s<=1;

end

else if(mss[7:0]==8'b10011001)

begin

mss[7:0]<=0;

mss[11:8]<=mss[11:8]+1;

end

else if(mss[3:0]==4'b1001)

begin

mss[3:0]<=0;

mss[7:4]<=mss[7:4]+1;

end

else

begin

mss[3:0]<=mss[3:0]+1;

clk\_1s<=0;

end

end

endmodule

**再以秒计数器为依据，设计count\_60,来实现分和小时**

module count\_60(

input clk,

input reset,

output reg [7:0] six\_ten,

output reg count\_carry

);

initial

begin

six\_ten<=8'b00000000;

count\_carry<=0;

end

always@(posedge clk)

begin

if(!reset)

begin

six\_ten<=8'b00000000;

count\_carry<=0;

end

if(six\_ten==8'b01011001)

begin

six\_ten<=8'b00000000;

count\_carry<=1;

end

else if(six\_ten[3:0]==4'b1001)

begin

six\_ten[3:0]<=4'b0000;

six\_ten[7:4]<=six\_ten[7:4]+1;

end

else

begin

six\_ten<=six\_ten+1;

count\_carry<=0;

end

end

Endmodule

最后设计天计数器：即count\_24

module count\_hour(

input clk,

input reset,

output reg [7:0] hour,

output reg count\_carry

);

initial

begin

hour<=8'b00000000;

count\_carry<=0;

end

always@(posedge clk)

begin

if(!reset)

begin

hour<=8'b00000000;

count\_carry<=0;

end

if(hour==8'b00100100)

begin

hour<=8'b00000000;

count\_carry<=1;

end

else if(hour[3:0]==4'b1001)

begin

hour[3:0]<=4'b0000;

hour[7:4]<=hour[7:4]+1;

count\_carry<=0;

end

else

begin

hour<=hour-1;

count\_carry<=0;

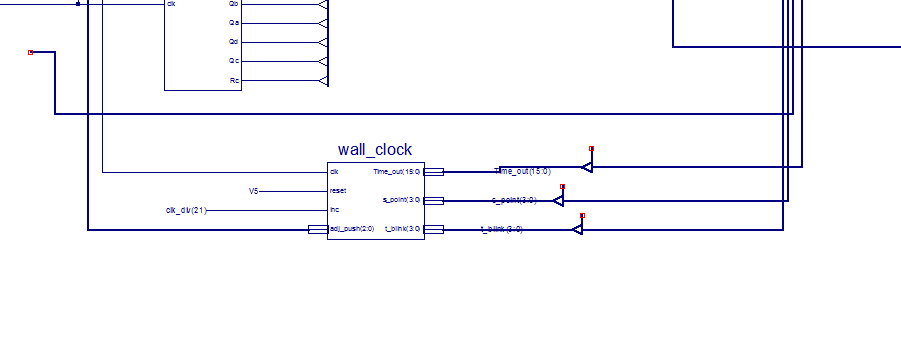
end

end

Endmodule

最后合成wall\_clock模块（见附件）

最后加入顶层模块：



下板之后结果见视频